In the Claims

1. (currently amended): A method for etching a layer of silicon nitride comprising:

etching said silicon nitride layer ~~in the absence of a photoresist layer~~ with an etchant consisting essentially of oxygen at a flow rate of between about 20 sccm and about 80 sccm and one of CHF_3 and CH_2F_2 at a flow rate of between about 5 sccm and about 25 sccm, wherein said flow rates provide an etch ~~etchant comprises at least~~ having proportions of greater than about 75% of said oxygen and less than about 25% of said one of CHF_3 and CH_2F_2; and

during said etching, subjecting said silicon nitride layer to a pressure of between about 10 millitorr and about 60 millitorr.

2. (original): The method of claim 1 further comprising introducing said oxygen and said one of CHF_3 and CH_2F_2 into an etch chamber at a ratio of about 3:1 during said etching.

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3. (previously amended): The method of claim 1 further comprising subjecting said silicon nitride layer to a power of between about 300 watts and about 600 watts during said etching.

4. (original): The method of claim 1 further comprising introducing said oxygen into an etch chamber at a flow rate of between about 35 sccm and about 60 sccm and introducing said one of CHF_3 and CH_2F_2 into said etch chamber at a flow rate of between about 10 and about 20 sccm during said etching.

5. (original): The method of claim 4 further comprising subjecting said silicon nitride layer to a pressure of between about 30 millitorr and 60 millitorr and a power of between about 300 watts and about 500 watts during said etching.

6. (original): The method of claim 1 further comprising introducing oxygen into an etch chamber at a flow rate of about 60 sccm and introducing said one of CHF_3 and CH_2F_2 into said etch chamber at a flow rate of about 20 sccm during said etching.

7. (original): The method of claim 6 further comprising subjecting said silicon nitride layer to a pressure of between about 30 and 40 millitorr and a power of between about 300 watts and about 400 watts during said etching.

8. (currently amended): A method used during the formation of a semiconductor device comprising:

providing a semiconductor wafer assembly comprising at least one of a layer of silicon and a layer of silicon dioxide;

forming a layer of silicon nitride over said at least one of said layer of silicon and said layer of silicon dioxide;

etching said silicon nitride ~~in the absence of a photoresist layer~~ with an etch consisting essentially of oxygen and one of CHF_3 and CH_2F_2 and a pressure of between about 10 millitorr and about 60 millitorr, wherein said flow rates provide an etch ~~comprises at least~~ having proportions of greater than about 75% of said oxygen and less than about 25% of said one of CHF_3 and CH_2F_2 and said etch exposes said at least one of said layer of silicon and said layer of silicon dioxide.

9. (currently amended): A method used during the formation of a semiconductor device comprising:

providing a semiconductor wafer assembly comprising a silicon wafer and a layer of silicon dioxide overlying said wafer;

forming a layer of silicon nitride over said silicon wafer and over said layer of silicon dioxide;

placing said semiconductor wafer assembly into an etch chamber;

etching said silicon nitride layer ~~in the absence of a photoresist layer~~ using an etch consisting essentially of oxygen and one of CHF_3 and CH_2F_2 and a pressure of between about 10 millitorr and about 60 millitorr to expose said silicon dioxide layer and said silicon wafer, wherein said flow rates provide an etch ~~comprises at least~~ having proportions of greater than about 75% of said oxygen and less than about 25% of said one of CHF_3 and CH_2F_2.

10. (original): The method of claim 9 further comprising introducing said oxygen and said one of CHF_3 and CH_2F_2 into said etch chamber at a ratio of about 3:1 during said etching.

11. (original): The method of claim 9 further comprising introducing oxygen into said chamber at a flow rate of between about 20 sccm and about 80 sccm and introducing said one of CHF_3 and CH_2F_2 into said etch chamber at a flow rate of between about 5 sccm and about 25 sccm during said etching.

12. (previously amended): The method of claim 11 further comprising subjecting said silicon nitride layer to a power of between about 300 watts and about 600 watts during said etching.

13. (original): The method of claim 9 further comprising introducing said oxygen into said chamber at a flow rate of between about 35 sccm and about 60 sccm and introducing said one of CHF_3 and CH_2F_2 into said etch chamber at a flow rate of between about 10 sccm and about 20 sccm during said etching.

14. (original): The method of claim 13 further comprising subjecting said silicon nitride layer to a pressure of between about 30 millitorr and 60 millitorr and a power of between about 300 watts and about 500 watts during said etching.

15. (original): The method of claim 9 further comprising introducing said oxygen into said chamber at a flow rate of about 60 sccm and introducing said one of CHF_3 and CH_2F_2 into said etch chamber at a flow rate of about 20 sccm during said etching.

16. (original): The method of claim 15 further comprising subjecting said silicon nitride layer to a pressure of between about 30 millitorr and 40 millitorr and a power of between about 300 watts and about 400 watts during said etching.

17. (new) A method of fabricating silicon nitride spacers on an integrated circuit device comprising:

providing a semiconductor substrate assembly comprising:

first and second vertically-oriented integrated circuit structures, each having a top and vertical surfaces, wherein said first and second integrated circuit structures are horizontally spaced from each other; and

a horizontal base surface interposed between said first and second integrated circuit structures;

forming a layer of silicon nitride over said top and vertical surfaces of each of said first and second integrated circuit structures such that said top and vertical surfaces of first and second integrated circuit structures and said horizontal base surface between said integrated circuit structures are covered with said layer of silicon nitride; and

anisotropically etching said layer of silicon nitride over said top surfaces of said first and second integrated circuit structures and over said horizontal base surface with an etchant consisting essentially of oxygen at a flow rate of between about 20 sccm to about 80 sccm and CHF_3 at a flow rate of between about 5 sccm to about 25 sccm, such that said flow rates of oxygen and CHF_3 have a ratio of about three to one (3:1) and provide a vertical to horizontal etch rate of about four to one (4:1) to result in silicon nitride spacers on said vertical integrated circuit structure.

18. (new) A method of fabricating silicon nitride spacers on an integrated circuit device comprising:

providing a semiconductor substrate assembly comprising:

first and second vertically-oriented integrated circuit structures, each having a top and vertical surfaces, wherein said first and second integrated circuit structures are horizontally spaced from each other; and

a horizontal base surface interposed between said first and second integrated circuit structures;

forming a layer of silicon nitride over said top and vertical surfaces of each of said first and second integrated circuit structures such that said top and vertical surfaces of first and second integrated circuit structures and said horizontal base surface between said integrated circuit structures are covered with said layer of silicon nitride; and

anisotropically etching said layer of silicon nitride over said top surfaces of said first and second integrated circuit structures and over said horizontal base surface with an etchant consisting essentially of oxygen at a flow rate of between about 20 sccm to about 80 sccm and CH_2F_2 at a flow rate of between about 5 sccm to about 25 sccm, such that said flow rates of oxygen to CH_2F_2 have a ratio of about three to one (3:1) and provide a vertical to horizontal etch rate of about four to one (4:1) to result in silicon nitride spacers on said vertical integrated circuit structure.